

Application No.: 10/690,463

Docket No.: JCLA12280

**In The Claims:**

Claim 1. (currently amended) A multi-finger transistor, comprising:  
a plurality of parallel gates on a substrate; ~~transistors, wherein each transistor comprises:~~  
a gate dielectric layer between the gates and the substrate; ~~and a gate on a substrate~~;  
a plurality of source/drain regions, each a source/drain region is formed in the substrate  
beside each the gate, wherein a region in the substrate under each gate is a channel region; and  
a plurality of drift region, each a drift region is formed in the peripheral substrate of  
between the each channel region and the each source/drain region separating the source/drain  
region and a channel region under the gate, wherein  
the drift regions in the central section of the multi-finger transistor surround the  
corresponding source/drain regions, and a width of the drift regions extending from a side  
boundary of the source/drain region to the boundary of the drift region along a direction parallel  
to the gate increases stepwise from the edge sections of the multi-finger transistor toward a the  
central section of the multi-finger transistor.

Claim 2. (currently amended) The multi-finger transistor of claim 1, wherein the multi-finger transistor is divided into  $2m+1$  sections along an arrangement direction of the parallel gates ~~transistors~~, wherein  $m$  is a positive integer, and the drift region extension width is smallest in the outmost sections of the multi-finger transistor and increases therefrom toward the central section of the multi-finger transistor.

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Claim 3. (original) The multi-finger transistor of claim 2, wherein  $m$  is 1 or 2.

Claim 4. (currently amended) The multi-finger transistor of claim 2, wherein the ~~drift~~  
~~region-extension~~ width is zero in the outmost sections of the multi-finger transistor.

Claim 5. (currently amended) The multi-finger transistor of claim 1, further comprising  
an isolation layer wherein the above each drift region of a transistor is located under an isolation  
layer, and the each gate of the same transistor partially covers the isolation layer.

Claim 6. (original) The multi-finger transistor of claim 5, wherein the isolation layer  
comprises a field oxide layer.

Claim 7. (currently amended) The multi-finger transistor of claim 1, wherein ~~two~~  
~~adjacent transistors share a source region or a drain region~~ the source or drain region beside one  
of the gate is connected with the source or drain region beside another gate.

Claim 8. (original) The multi-finger transistor of claim 7, wherein a width of the drain  
region is larger than a width of the source region.

Claim 9. (currently amended) A multi-finger transistor, comprising:  
a plurality of parallel gates on a substrate, wherein the substrate further has a pick-up  
region thereon; transistors, wherein each transistor comprises;

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a gate dielectric layer between the gates and the substrate; and a gate on a substrate,  
~~wherein the substrate further has a pick-up region thereon;~~

a plurality of source/drain regions, each a source/drain region is formed in the substrate  
beside each the gate, wherein a region in the substrate under each gate is a channel region; and

a plurality of drift region, each a drift region is formed in the ~~peripheral~~ substrate of  
between the each channel region and the each source/drain region-separating the source/drain  
~~region and a channel region under the gate,~~ wherein

the drift regions in the central section of the multi-finger transistor surround the  
corresponding source/drain regions, and a width of ~~the drift regions extending~~ from a side  
boundary of the source/drain region to the boundary of the drift region along a direction parallel  
to the gate increases with an increase in a distance between ~~the transistor~~ each gate and the pick-  
up region.

Claim 10. (currently amended) The multi-finger transistor of claim 9, further comprising  
an isolation layer wherein the above each drift region of a transistor is located under an isolation  
layer, and the each gate of the same transistor partially covers the isolation layer.

Claim 11. (original) The multi-finger transistor of claim 10, wherein the isolation layer  
comprises a field oxide layer.

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Claim 12. (currently amended) The multi-finger transistor of claim 9, wherein ~~two adjacent transistors share a source region or a drain region~~ the source or drain beside one of the gate is connected with the drain or source beside another gate.

Claim 13. (original) The multi-finger transistor of claim 12, wherein a width of the drain region is larger than a width of the source region.